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In re Application of:

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For:   BROADCASTING SIGNAL RECEIVER APPARATUS PROVIDED
       WITH CONTROLLER FOR CONTROLLING DEMODULATION MODE,
       AND APPARATUS FOR CONTROLLING DEMODULATION MODE

## TRANSLATOR'S DECLARATION

Commissioner for Patents

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Sir:

     I, Kazuhiko YASUI of c/o AOYAMA & PARTNERS, 3-7, Shiromi 1-chome, Chuo-ku, Osaka-shi, Osaka 540-0001 Japan, declare:

     that I am thoroughly familiar with both the Japanese and English languages;

     that the attached document represents an accurate English translation of U.S. Patent Application Serial No. 10/829,189 as filed April 22, 2004; and

     that I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: August 26, 2004

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                                            Kazuhiko YASUI

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TITLE OF THE INVENTION

Broadcasting Signal Receiver Apparatus Provided With Controller For Controlling Demodulation Mode, And Apparatus For Controlling Demodulation Mode

5    BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to a broadcasting signal receiver apparatus and a demodulation mode.   More specifically, the present invention relates to a broadcasting signal receiver apparatus which

10    receives a broadcasting signal of, for example, a cable television (referred to as a CATV hereinafter), and an apparatus for controlling a demodulation mode for controlling the demodulation mode upon demodulating a modulated received signal such as the broadcasting signal or the like.

15    2. DESCRIPTION OF THE RELATED ART

In recent years, following the progress of video digitalization, every country has started digital broadcasting through broadcasting media of satellite broadcasting, CATV broadcasting, and terrestrial broadcasting. Various kinds of transmission systems have been proposed as those

20    suited for features of respective transmission lines.   In particular, in the CATV broadcasting, various kinds of services such as a pay-per-view service or the like are provided taking advantage of stability and an interactiveness of the transmission line.   According to a conventional CATV broadcasting system, an individual transmission system including

25    a conditional access (referred to as a CA hereinafter) is adopted for each network operator, that is, each CATV broadcasting entity.   Due to this, a manufacturer manufactures a set-top box (referred to as an STB hereinafter) and supplies the STB to each network operator based on

standards of the network operator.   A viewer concludes a viewing contract with each network operator and leases the STB from the network operator.

In these circumstances, in North America where 70% or more of

5    TV viewers receive broadcasting programs through CATV, standards of separating apparatus parts such as the CA depending on each network operator from the STB for the CATV is disclosed by, for example, specifications for OpenCable (trademark), i.e., a prior-art technical literature of Cable Television Laboratories, Inc.: OpenCable™ Host Device

10    Core Functional Requirements, Issued Specification, OC-SP-HOST-CFR-I10-020628, pp. 1-47, updated on June 28, 2002, http://www.opencable.com/specifications/ as issued by Cable Television Laboratories, Inc for promotion of making STB's for CATV marketable. Based on the standards, each manufacturer is capable of making the

15    CATV STB marketable integrally with a television receiver, a DVD player, a DVD recorder, or the like.   In addition, the number of choices of products increases for consumers.

A security card which is provided depending on the network operator and which stores security information on each network operator

20    and broadcasting signals from the network operator and a control program is mounted into the STB as disclosed by the prior art document. The security card is also referred to as a point of deployment (POD) module or cable card.   When a viewer having this STB sees a toll broadcasting program, the viewer inserts the security card into the STB.

25    Then, the security card generates a descrambling key based on CA information, and outputs the descrambling key to the STB.   The STB descrambles and MPEG-decodes data on a toll broadcasting signal based on the inputted descrambling key, and acquires a video signal and a voice

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signal.

However, a viewer who sees only toll-free broadcasting programs does not necessarily mount the security card into the STB. If so, it disadvantageously takes a lot of time to select a channel for the

5    broadcasting signal.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a broadcasting signal receiver apparatus which can solve the disadvantages, and which enables selecting a desired channel for a broadcasting signal more quickly

10   even if a viewer who sees only toll-free broadcasting programs or the like does not mount a security card into a set-top box, and an apparatus for controlling a demodulation mode for the broadcasting signal receiver apparatus or the like.

According to a first aspect of the present invention, there is

15   provided a broadcasting signal receiver apparatus including a security device and a receiver. The security device stores security information on a broadcasting entity, and extracts transmission information for receiving a broadcasting signal modulated in a predetermined modulation mode from a control signal transmitted from an apparatus of the broadcasting

20   entity. The receiver receives the broadcasting signal transmitted from the apparatus of the broadcasting entity based on the extracted transmission information. The security device is separated from the receiver, and can be mounted in the receiver. The broadcasting signal receiver apparatus further includes a tuner, a demodulator, a first

25   controller, a synchronization judgment unit, a device detector, and a second controller. The tuner controls a frequency of the received broadcasting signal to select a channel of a predetermined broadcasting signal. The demodulator is capable of demodulating the broadcasting

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signal transmitted from the apparatus of the broadcasting entity in a plurality of demodulation modes corresponding to modulation modes of modulation systems of the broadcasting signal, and the demodulator demodulates the broadcasting signal of the channel selected by the tuner

5    in a demodulation mode which is set among the plurality of demodulation modes.   The first controller controls the demodulation mode of the demodulator, and the synchronization judgment unit judges whether or not the demodulator is synchronized with the received broadcasting signal, and outputs a synchronization judgment result signal.   The device

10    detector detects whether or not the security device is mounted into the receiver.   When the device detector detects that the security device is not mounted into the receiver, the second controller controls the tuner, the demodulator, and the first controller, so as to change at least one of the demodulation mode for the broadcasting signal and the frequency of the

15    broadcasting signal, and to retrieve the broadcasting channel on which the transmission information on the broadcasting signal is transmitted. Then the second controller receives the broadcasting signal on the retrieved broadcasting channel.   When the synchronization judgment unit judges that the demodulator is synchronized with the broadcasting

20    signal, the second controller extracts the transmission information on the broadcasting channel from the broadcasting signal demodulated by the demodulator, and receives the broadcasting signal based on the extracted transmission information on the broadcasting signal.

In the above-mentioned broadcasting signal receiver apparatus,

25    the second controller initializes a demodulation mode control processing executed by the first controller immediately after the frequency of the tuner is changed.

Also, in the above-mentioned broadcasting signal receiver

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apparatus, the first controller controls at least one of a modulation rate, filter coefficients, and a constellation which are set to the demodulator based on the synchronization judgment result signal from the synchronization judgment unit until the demodulator is synchronized

5    with the received broadcasting signal.

Further, in the above-mentioned broadcasting signal receiver apparatus, the demodulator includes a carrier recovery circuit which reproduces a carrier wave of the received broadcasting signal, and the synchronization judgment unit judges whether or not the demodulator is

10    synchronized with the received broadcasting signal based on a phase error of a signal reproduced by the carrier recovery circuit.

Further, in the above-mentioned broadcasting signal receiver apparatus, the demodulator includes a clock recovery circuit which reproduces a clock signal of the received broadcasting signal, and the

15    synchronization judgment unit judges whether or not the demodulator is synchronized with the received broadcasting signal based on a phase error of the clock signal reproduced by the clock signal recovery circuit.

Further, in the above-mentioned broadcasting signal receiver apparatus, the demodulator includes an error correction circuit which

20    corrects an error of the received broadcasting signal, and the synchronization judgment unit judges whether or not the demodulator is synchronized with the received broadcasting signal based on whether or not a frame synchronous signal outputted from the error correction circuit can be detected.

25    Still further, in the above-mentioned broadcasting signal receiver apparatus, each of the first controller and the synchronization judgment unit is constituted by a hardware circuit.

According to a second aspect of the present invention, there is

provided an apparatus for controlling a demodulation mode including a demodulator, a controller, and a synchronization judgment unit.   The demodulator is capable of demodulating a received signal modulated in a predetermined modulation mode, in a plurality of demodulation modes

5   corresponding to modulation modes of modulation systems of the received signal, and the demodulator demodulates the received signal in a demodulation mode which is set among the plurality of demodulation modes.   The controller controls the demodulation mode of the demodulator, and the synchronization judgment unit judges whether or

10   not the demodulator is synchronized with the received signal, and outputs a synchronization judgment result signal.   The controller controls the demodulation mode of the demodulator based on the synchronization judgment result signal from the synchronization judgment unit until the demodulator is synchronized with the received signal.

15   Also, in the above-mentioned apparatus for controlling a demodulation mode, the controller controls at least one of a modulation rate, filter coefficients and a constellation which are set to the demodulator based on the synchronization judgment result signal from the synchronization judgment unit until the demodulator is synchronized

20   with the received signal.

Further, in the above-mentioned apparatus for controlling a demodulation mode, the demodulator includes a carrier recovery circuit which reproduces a carrier wave of the received signal, and the synchronization judgment unit judges whether or not the demodulator is

25   synchronized with the received signal based on a phase error of a signal reproduced by the carrier recovery circuit.

Further, in the above-mentioned apparatus for controlling a demodulation mode, the demodulator includes a clock recovery circuit

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which reproduces a clock signal of the received signal, and the synchronization judgment unit judges whether or not the demodulator is synchronized with the received signal based on a phase error of the clock signal reproduced by the clock recovery circuit.

5        Further, in the above-mentioned apparatus for controlling a demodulation mode, the demodulator includes an error correction circuit which corrects an error of the received signal, and the synchronization judgment unit judges whether or not the demodulator is synchronized with the received signal based on whether or not a frame synchronous

10    signal outputted from the error correction circuit can be detected.

Still further, in the above-mentioned apparatus for controlling a demodulation mode, each of the controller and the synchronization judgment unit is constituted by a hardware circuit.

According to the broadcasting signal receiver apparatus according

15    to the present invention, when the device detector detects that the security device is not mounted into the receiver, the tuner, the demodulator and the first controller are controlled so as to change at least one of the demodulation mode for the broadcasting signal and the frequency of the broadcasting signal, and to retrieve the broadcasting

20    channel on which the transmission information on the broadcasting signal is transmitted.  Then, the broadcasting signal on the retrieved broadcasting channel is received.  When the synchronization judgment unit judges that the demodulator is synchronized with the broadcasting signal, the transmission information on the broadcasting channel is

25    extracted from the broadcasting signal demodulated by the demodulator, and the broadcasting signal is received based on the extracted transmission information on the broadcasting signal.  Accordingly, even if a viewer who sees only toll-free broadcasting programs or the like does

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not mount the security card into the set-top box, a desired channel for a broadcasting signal can be selected more quickly.

Further, according to the apparatus for controlling a demodulation mode according to the present invention, the demodulation mode of the

5    demodulator is controlled based on the synchronization judgment result signal from the synchronization judgment unit until the demodulator is synchronized with the received signal. Accordingly, the demodulation mode of the received signal can be detected and controlled more certainly at a higher speed, as compared with the prior art.

10    BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and features of the present invention will become clear from the following description taken in conjunction with the preferred embodiments thereof with reference to the accompanying drawings throughout which like parts are designated by like reference

15    numerals, and in which:

Fig. 1 is a block diagram showing a configuration of a set-top box 100 and a security card 200 for receiving a CATV broadcasting signal, according to a preferred embodiment of the present invention;

Fig. 2 is a block diagram showing a configuration of a QAM

20    demodulator 12, a demodulation mode controller 17, and a synchronization judgment circuit 16 shown in Fig. 1;

Fig. 3 is a diagram showing a demodulation mode table stored in a data memory 23m shown in Fig. 1;

Fig. 4 is a flowchart showing an initial operation processing

25    executed by an apparatus controller 23 shown in Fig. 1;

Fig. 5 is a flowchart showing an FAT channel transmission information acquisition processing (step S2) which is a subroutine of the processing shown in Fig. 4;

Fig. 6 is a flowchart showing an FAT channel retrieve processing (step S3) which is a subroutine of the processing shown in Fig. 4;

Fig. 7 is a block diagram showing a configuration of a carrier recovery circuit 123A and a synchronization judgment circuit 16A
5 according to a first modified preferred embodiment of the present invention;

Fig. 8 is a block diagram showing a clock recovery and sampling circuit 121A and a synchronization judgment circuit 16B according to a second modified preferred embodiment of the present invention; and

10 Fig. 9 is a diagram showing an arrangement of channels used by a CATV for the set-top box 100 shown in Fig. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments according to the present invention will be described below with reference to the attached drawings.   Components
15 similar to each other are denoted by same reference, respectively.

Fig. 1 is a block diagram showing a configuration of a set-top box (STB) 100 and a security card 200 for receiving a CATV broadcasting signal, according to a preferred embodiment of the present invention. The security card 200 is a security device that stores security information
20 on a CATV broadcasting entity and on broadcasting signals transmitted from a head end apparatus of the CATV broadcasting entity, and that stores a control program for extracting transmission information for receiving a broadcasting channel signal from a control signal transmitted from the head end apparatus of the company.   The security card 200 is
25 mounted into a slot 200S of the STB 100 according to the present preferred embodiment.   In this case, since the security card 200 executes signal processings dependent on the broadcasting entity, the security card 200 is also referred to as a POD module.

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Referring to Fig. 1, the STB 100 includes an RF terminal 10, a QAM tuner 11, a QAM demodulator 12, a demodulation mode controller 17, a synchronization judgment circuit 16, a tuner frequency controller 18, a QPSK tuner 13, a QPSK demodulator 14, a QPSK modulator 15, a

5      switch 20, an MPEG (Moving Picture Experts Group) demodulator 21, a descrambler 22, and an apparatus controller 23 including a data memory 23m. The STB 100 according to the present preferred embodiment is characterized particularly by including the demodulation mode controller 17 for controlling a demodulation mode of the QAM demodulator 12, the

10     synchronization judgment circuit 16 which executes a synchronization judgment based on an output signal from the QAM demodulator 12, and the tuner frequency controller 18 for controlling a tuning frequency of the QAM tuner 11.

Referring to Fig. 1 again, signals inputted and outputted through

15     the RF terminal 10 are generally classified to signals on the following three types of channels, which enable an interactive service. The signals on the three types of channels are transmitted respectively through divided frequency bands shown in Fig. 9.

Referring to Fig. 9, a first channel is a channel in a frequency band

20     from 54 to 864 MHz, for transmitting an application-related broadcasting signal such as a video signal and a voice signal with a frequency band of 6 MHz per channel. The first channel is referred to as an FAT channel (Forward Application Transport Channel). The broadcast signal on the first channel is modulated according to a 256QAM or 64QAM digital

25     modulation system. A second channel is a channel in a frequency band from 70 to 130 MHz, for transmitting service information (SI) and conditional access (CA) for reception of an FAT channel with a frequency band of 1 to 2 MHz per channel. The second channel is referred to as an

FDC channel (Forward Data Channel). A control signal on the second channel is digital-modulated according to a QPSK modulation system. A third channel is a channel in a frequency band of 5 to 42 MHz, for transmitting request information from a broadcasting signal receiver

5    apparatus such as the STB to a head end with a frequency band of 1 to 2 MHz per channel. The third channel is referred to as an RDC channel (Reverse Data Channel). A control signal on the third channel is QPSK-modulated to a digital signal.

Respective signal processings for the signals on the three types of

10    channels inputted and outputted through the RF terminal 10 will be described below.

Broadcasting signals on the FAT channel are inputted to the STB through the RF terminal 10. Thereafter, the QAM tuner 11 extracts only one desired broadcasting signal among a plurality of QAM-modulated

15    broadcasting signals present in the frequency band from 54 to 864 MHz, and outputs the extracted broadcasting signal to the QAM demodulator 12. The QAM demodulator 12 can demodulate broadcasting signals received in a plurality of demodulation modes corresponding to modulation systems of the demodulated broadcasting signals. The QAM

20    demodulator 12 carries out processings such as clock recovery, automatic gain control, carrier recovery, waveform equalization, and error correction or the like on the inputted QAM-modulated broadcasting signal, demodulates the FAT data in the demodulation mode of the demodulation system corresponding to the modulation system of the modulated

25    broadcasting signal, and outputs the demodulated FAT data to the switch 20. The switch 20 is controlled by the apparatus controller 23 to be selectively switched over to a contact "a" or a contact "b". When the security card 200 is mounted into the slot 200S of the STB 100, the

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switch 20 is switched over to the contact "b".   The FAT data from the
QAM demodulator 12 is outputted to the security card 200.   When the
security card 200 is not mounted into the slot 200S of the STB 100, the
switch 20 is switched over to the contact "a".   The FAT data from the
5   QAM demodulator 12 is outputted to the MPEG decoder 21.

When the security card 200 is mounted into the slot 200S of the
STB 100, the security card 200 generates a descrambling key based on
FDC data or a CA information extracted from the FAT data, and outputs
the descrambling key to the descrambler 22.   The descrambler 22
10   descrambles the toll FAT data based on the descrambling key, and
outputs the descrambled FAT data to the MPEG decoder 21.   The MPEG
decoder 21 MPEG-decodes the FAT data inputted from the switch 20 or
the FAT data inputted from the descrambler 22, so as to reproduce and
output the video and voice signals.   When the security card 200 is not
15   mounted into the slot 200S of the STB 100, the switch 20 is switched over
to the contact "a".   The FAT data from the QAM demodulator 12 is
inputted to the MPEG decoder 21.   When the FAT data is not scrambled,
the MPEG decoder 21 executes an MPEG decoding processing to the FAT
data.

20   The FDC data is inputted to the QPSK tuner 13 through the RF
terminal 10.   The QPSK tuner 13 extracts a QPSK-modulated control
signal in the frequency band from 70 to 130 MHz, and outputs the
extracted control signal to the QPSK demodulator 14.   The QPSK
demodulator 14 carries out processings such as clock recovery, automatic
25   gain control, carrier recovery, waveform equalization, and error correction
or the like on the inputted QPSK-modulated control signal, demodulates
the FDC data, and outputs the demodulated FDC data to the security
card 200.   In response to this, the security card 200 extracts SI

information and CA information for FAT channel reception based on the FDC data outputted from the QPSK demodulator 14.

Further, the RDC data is generated by the security card 200, and is inputted to the QPSK modulator 15. The QPSK modulator 15

5    QPSK-modulates a control signal according to the inputted RDC data, and outputs the QPSK-modulated control signal to the QPSK tuner 13. The QPSK tuner 13 subjects the inputted control signal to a frequency conversion so as to convert a frequency of the control signal to a frequency in the frequency band from 5 to 42 MHz, and transmits the

10    frequency-converted control signal to the head end apparatus of the broadcasting entity through the RF terminal 10.

Fig. 2 is a block diagram showing a configuration of the QAM demodulator 12, the demodulation mode controller 17, and the synchronization judgment circuit 16 shown in Fig. 1. Referring to Fig. 2,

15    the QAM demodulator 12 includes an input terminal 120, a clock recovery and sampling circuit 121, a roll-off filter 122, a carrier recovery and waveform equalization circuit 123, an error correction circuit 124, and an output terminal 125. The demodulation mode controller 17 includes a baud rate controller 170, a filter coefficient controller 171, a constellation

20    controller 172, and a controller 173.

A basic operation of the QAM demodulator 12 will be first described. The QAM-modulated signal inputted through the input terminal 120 is first inputted to the clock recovery and sampling circuit 121. The clock recovery and sampling circuit 121 reproduces a clock

25    signal synchronized in phase with a modulation clock of the received QAM-modulated signal at a predetermined baud rate, that is, reproduces the clock signal with which the QAM-modulated signal can be sampled at coding points of the QAM constellation. In addition, the clock recovery

and sampling circuit 12 samples the inputted QAM-modulated signal based on the reproduced clock signal, and outputs the sampled QAM-modulated signal to the carrier recovery and waveform equalization circuit 123 through the roll-off filter 122 for performing a band limitation

5    at predetermined roll-off coefficients. The carrier recovery and waveform equalization circuit 123 reproduces a carrier wave synchronized in phase with a carrier wave of the inputted QAM-modulated signal using a constellation according to a predetermined modulation system. The carrier recovery and waveform equalization circuit 123 removes a phase

10    deviation and a frequency deviation of the inputted QAM-modulated signal based on the reproduced carrier wave, and removes a reflection component contained in the inputted QAM-modulated signal. Then, the carrier recovery and waveform equalization circuit 123 outputs an output signal to the error correction circuit 124. The error correction circuit 124

15    decodes an error correction code encoded on a transmission side for the output signal from the carrier recovery and waveform equalization circuit 123 inputted to the error correction circuit 124. Then the error correction circuit 124 corrects a bit error due to a noise or the like on a transmission line, and outputs error-corrected data through the output

20    terminal 125 as the FAT data.

A demodulation mode control processing will be described.

The baud rate controller 170 is controlled by the controller 173, and is connected with the clock recovery and sampling circuit 121 of the QAM demodulator 12. The baud rate controller 170 sets a baud rate

25    corresponding to the QAM-modulated signal which is likely to be received as an initial value of a phase synchronization loop for the clock recovery, to the clock recovery and sampling circuit 121. The clock recovery and sampling circuit 121 calculates an error between the set baud rate and

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the baud rate of the received QAM-modulated signal, so as to reproduce the clock signal.

The filter coefficient controller 171 is controlled by the controller 173, and is connected with the roll-off filter 122 of the QAM demodulator

5   12. The filter coefficient controller 171 sets filter coefficients corresponding to the QAM-modulated signal which is likely to be received, to the roll-off filter 122. The constellation controller 172 is controlled by the controller 173, and is connected with the carrier recovery and waveform equalization circuit 123 of the QAM demodulator 12. The

10  constellation controller 172 sets an ideal constellation corresponding to the QAM-modulated signal which is likely to be received, to the carrier recovery and waveform equalization circuit 123. The carrier recovery and waveform equalization circuit 123 calculates an error between the set ideal constellation and a constellation of the received QAM-modulated

15  signal, so as to carry out the carrier recovery and waveform equalization processings.

The synchronization judgment circuit 16 judges whether or not the QAM demodulator 12 can be synchronized with the received QAM-modulated signal based on whether or not a synchronous signal (a

20  unique word) in a specific frame among transmitted frames of the QAM-modulated signal can be detected based on the output signal from the error correction circuit 124 of the QAM demodulator 12. The synchronization judgment circuit 16 outputs a synchronization judgment result signal to the controller 173, the tuner frequency controller 18, and

25  the apparatus controller 23.

The controller 173 controls the baud rate controller 170, the filter coefficient controller 171 and the constellation controller 172 based on the synchronization judgment result signal of the QAM demodulator 12

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outputted from the synchronization judgment circuit 16. For example, if the demodulation mode to the QAM-modulated signal which is likely to be received includes a plurality of demodulation modes (MODE) in the demodulation mode table stored in the data memory 23m and shown in

5    Fig. 3, the controller 173 sets the baud rate (which is not limited to the baud rate according to the present invention, and which may be a modulation rate such as a symbol rate corresponding to the modulation system of the modulated broadcasting signal, which can be applied to the below embodiments), the roll-off coefficients, and the constellation

10    corresponding to a modulation format, corresponding to the demodulation system in, for example, a demodulation mode MODE = 0 (where the demodulation system will be referred to as a demodulation system corresponding to the modulation system of the modulated broadcasting signal), to the clock recovery and sampling circuit 121, the roll-off filter

15    122, and the carrier recovery and waveform equalization circuit 123 of the QAM demodulator 12, respectively. Then, if the QAM demodulator 12 cannot be synchronized with the input signal for a predetermined period of time, the controller 173 instructs the baud rate controller 170, the filter coefficient controller 171, and the constellation controller 172 to switch

20    the baud rate, the roll-off coefficients, and the constellation corresponding to the modulation format thus set to a baud rate, roll-off coefficients, and a constellation corresponding to the modulation format corresponding to a setting different from the previous setting, e.g., a demodulation system in a demodulation mode MODE=1, respectively.

25        As described above, since the demodulation mode is detected and controlled based on the synchronization result of the QAM demodulator 12, the demodulation mode control can be executed more certainly at a higher speed.

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In the present preferred embodiment, the synchronization judgment circuit 16 judges whether or not the QAM demodulator 12 is synchronized with the QAM-modulated signal based on whether or not the synchronous signal (the unique word) in the specific frame among

5      transmitted frames can be detected based on the output signal from the error correction circuit 124.   Alternatively, a synchronization judgment method other than this method may be used, which will be described later in detail.

        Fig. 4 is a flowchart showing an initial operation processing

10     executed by the apparatus controller 23 shown in Fig. 1.   The initial operation processing is executed, for example, when the STB 100 is initially disposed, or when a power is turned on.   Referring to Fig. 4, at step S1, it is judged whether or not the security card 200 is mounted into the slot 200S.   If the judgment result is YES, the control flow goes to step

15     S2.   If the judgment result is NO, the control flow goes to step S3.   At step S2, after executing an FAT channel transmission information acquisition processing shown in Fig. 5, the initial operation processing is finished.   At step S3, after executing an FAT channel retrieve processing shown in Fig. 6, the initial operation processing is finished.

20         Fig. 5 is a flowchart showing an FAT channel transmission information acquisition processing (the step S2) which is a subroutine of the processing shown in Fig. 4.   In the FAT channel reception, it is necessary to know which frequency in the frequency band from 54 to 864 MHz in which modulation system the broadcasting signal is transmitted.

25     The SI information as information necessary for this end is transmitted with the FDC data.   Prior to reception of the FAT channel, the STB 100 extracts FAT channel transmission information from FDC channels under control of the security card 200 as an initial operation.

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Referring to Fig. 5, at step S11, an FDC channel which corresponds to a frequency of the FDC data is retrieved in a frequency band from 70 to 130 MHz.   At step S12, the SI information is acquired from the retrieved FDC data.   At step S13, the FAT channel transmission

5    information is extracted from the acquired SI information.   At step S14, the acquired FAT channel transmission information is transmitted to the apparatus controller 23 of the STB 100, and the control flow returns to the original main routine.   By executing the processing shown in Fig. 5, later FAT channel reception is possible.

10    Fig. 6 is a flowchart showing an FAT channel retrieve processing (the step S3) which is a subroutine of the processing shown in Fig. 4.   It is assumed in Fig. 6 that a frequency channel number on the FAT channels is $f_n$, and that the channel number $f_n$ ranges from channel numbers 1 to $f_{max}$.

15    Referring to Fig. 6, at step S21, the apparatus controller 23 instructs the tuner frequency controller 18 to set a selected frequency of the QAM tuner 11 to a certain initial frequency.   Namely, the channel number $f_n$ is initialized to one.   When the frequency setting for the QAM tuner 11 is completed, the apparatus controller 23 controls the

20    demodulation mode controller 17 to set the demodulation mode (MODE) of the QAM demodulator 12 to zero at step S22.   Namely, the demodulation mode (MODE) is initialized to zero.   At step S23, the synchronization judgment circuit 16 judges whether or not the QAM demodulator 12 is synchronized with the QAM-modulated signal.   If the

25    judgment result is YES, the control flow goes to step S24.   If the judgment result is NO, the control flow goes to step S31.   At step S31, the apparatus controller 23 controls the demodulation mode controller 17 to increment the waiting demodulation mode (MODE) of the QAM

demodulator 12 by one.   At step S32, it is judged whether or not the modulation mode (MODE) is two or more.   If the judgment result is YES, the control flow goes to step S33.   If the judgment result is NO, the control flow returns to the step S23, and then, the processing of the step

5    S23 is executed.   At step S33, the channel number $f_n$ is incremented by one.   At step S34, it is judged whether or not the channel number $f_n$ is larger than the maximum channel number $f_{max}$.   If the judgment result is YES, the control flow goes to step S35.   If the judgment result is NO, the control flow returns to the step S22.   At step S35, an error processing is

10    executed, information on the demodulation system corresponding to the modulation system and the like, i.e., information as to presence or absence of respective channels obtained by the channel retrieve executed so far and the modulation system with which the QAM demodulator 12 can be synchronized, in the data memory 23m.   Then the control flow

15    returns to the original main routine.

　　　　　At step S24, the FAT channel transmission information is acquired from the FAT data.   At step S25, it is judged whether or not the FAT channel transmission information can be acquired at step S24.   If the judgment result is YES, the control flow goes to step S26.   If the

20    judgment result is NO, the control flow goes to step S33.   At step S26, the FAT channel transmission information is stored in the data memory 23m of the apparatus controller 23, then an FAT channel signal is received based on the FAT channel transmission information, and the control flow returns to the original main routine.

25    　　　　　As described above, even if the viewer who sees only toll-free broadcasting programs does not mount the security card 200 into the slot 200S of the STB 100, then the FAT channel transmission information can be acquired, and the desired FAT channel can be received at a higher

speed with higher efficiency from among a plurality of FAT channels in the frequency band from 54 to 864 MHz, by allowing the STB 100 to execute the initial operation processing shown in Fig. 6 prior to reception of the FAT channel.

5        In the preferred embodiment as described above, the content of the demodulation mode table shown in Fig. 3 is given only as one example, and various other baud rates (including modulation rates such as symbol rates or the like) and various other roll-off coefficients can be used. Further, only two demodulation modes are described in the demodulation

10    mode table shown in Fig. 3.    Alternatively, the constellation of the modulation system, the modulation rate such as the baud rate or the like, and the roll-off coefficients may be individually controlled until the QAM demodulator 12 is synchronized with the received QAM-modulated signal. Alternatively, at least one of the constellation of the modulation system,

15    the modulation rate such as the baud rate or the like, and the roll-off coefficients may be controlled until the QAM demodulator 12 is synchronized with the received QAM-modulated signal.

        In the preferred embodiment as described above, the demodulation mode controller 17, the synchronization judgment circuit 16, and the

20    tuner frequency controller 18 are each constituted by hardware circuits. Alternatively, each of the demodulation mode controller 17, the synchronization judgment circuit 16, and the tuner frequency controller 18 may be constituted by software using, for example, MPU or DSP. However, it is noted that by constituting each of the demodulation mode

25    controller 17, the synchronization judgment circuit 16, and the tuner frequency controller 18 by the hardware, a communication time of the apparatus controller 23 can be shortened, and the processing can be executed at a higher speed.

Fig. 7 is a block diagram showing a configuration of a carrier recovery circuit 123A and a synchronization judgment circuit 16A according to a first modified preferred embodiment of the present invention.   The first modified preferred embodiment is characterized by

5   executing a synchronization judgment based on a phase error generated after carrier recovery.   In Fig. 7, the carrier recovery circuit 123A includes a complex multiplier 51, a phase error detector 52, a low-pass filter (LPF) 53, and a numeric control oscillator (NCO) 54.

Referring to Fig. 7, the digital modulated signal subjected to

10   waveform shaping by the roll-off filter 122 is inputted to the complex multiplier 51.   It is assumed herein that a frequency error (or frequency deviation) $\Delta\omega$ and a phase error (or phase deviation) $\Delta\theta$ of this digital signal (referred to as an input signal hereinafter) Sin remain therein. Then in the I and Q axes orthogonal to each other, an in-phase signal

15   component of the input signal Sin on an I axis is set to Si, and an orthogonal signal component of the input signal Sin on a Q axis is set to Sq.   In this case, the input signal Sin is represented by the following Equation (1):

$$Sin = (Si + jSq) \cdot \exp(j(\Delta\omega t + \Delta\theta)) \qquad \ldots\ldots \quad (1).$$

20   The NCO 54 outputs an oscillation signal $S_{NCO}$, which is conjugate with a carrier wave signal $\exp(j(\Delta\omega t + \Delta\theta))$ of the input signal Sin represented by the Equation (1).   The oscillation signal $S_{NCO}$ is represented by the following Equation (2):

$$S_{NCO} = \exp(-j(\Delta\omega t + \Delta\theta)) \qquad \ldots\ldots \quad (2).$$

25   The complex multiplier 51 performs a complex multiplication between the oscillation signal $S_{NCO}$ from the NCO 54 and the input signal Sin, so as to remove the frequency error $\Delta\omega$ and the phase error $\Delta\theta$ of the input signal Sin, and then, outputs a demodulated signal Sout = (Si + jSq)

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as represented by the following Equation (3):

Sout

$= (Si + jSq) \cdot \exp(j(\Delta\omega t + \Delta\theta)) \cdot \exp(-j(\Delta\omega t + \Delta\theta))$

$= (Si + jSq)$  ...... (3).

5    The demodulated signal Sout from the complex multiplier 51 is

also inputted to the phase error detector 52. The phase error detector 52

detects the phase error of the received digital modulated signal from a real

part Si and an imaginary part Sq of the demodulated signal Sout based

on the control signal being transmitted from the constellation controller

10   172 and indicating the constellation. An output signal from the phase

error detector 52 is inputted to the LPF 53 of a loop filter. The LPF 53

removes a high frequency component of the phase error, and inputs the

resultant phase error to the NCO 54 as a control signal. The oscillation

signal $S_{NCO}$ from the NCO 54 controlled by an output signal from the LPF

15   53 is supplied to the complex multiplier 51.

As represented by the Equations (1) and (2), if the oscillation

signal $S_{NCO}$ from the NCO 54 is conjugate with the carrier wave signal of

the input signal Sin, that is, the input signal Sin includes no frequency

error $\Delta\omega$ and no phase error $\Delta\theta$, the phase error detected by the phase

20   error detector 52 is zero. However, if the phase difference is present

between the Equations (1) and (2), then the phase error detector 52

detects the phase error, and outputs a voltage corresponding to the phase

error to the NCO 54 through the LPF 53.

The synchronization judgment circuit 16A time-averages the

25   output signal being transmitted from the phase error detector 52 and

indicating the phase error, and compares the average phase error with a

predetermined threshold value. If the average phase error is smaller

than the threshold value, then the synchronization judgment circuit 16A

judges that the QAM demodulator 12 is synchronized with the QAM-modulated signal, and outputs a synchronization judgment result signal to the demodulation mode controller 17, the tuner frequency controller 18, and the apparatus controller 23 shown in Fig. 1,

5    respectively.

In the carrier recovery circuit 123A shown in Fig. 7, a negative feedback control loop is constituted so as to cancel the phase error detected by the phase error detector 52.   Therefore, a carrier wave synchronized in phase with the received digital modulated signal is

10    reproduced by the NCO 54.   This reproduced carrier wave is conjugate with the carrier wave signal of the input signal Sin, and the input signal Sin includes no frequency error $\Delta\omega$ and no phase error $\Delta\theta$.   Accordingly, an accurate demodulated signal can be acquired.

By the way, if the constellation indicated by the control signal

15    outputted from the constellation controller 172 coincides with the received digital modulated signal, then the phase error detector 52 can accurately detect the phase error, and the negative feedback control loop functions so as to cancel the phase error.   Therefore, the phase error detected by the phase error detector 52 becomes zero, finally.   However, if

20    the constellation indicated by the control signal outputted from the constellation controller 172 does not coincide with the received digital modulated signal, then the phase error detector 52 cannot detect an accurate phase error, and the negative feedback control loop does not normally operate.   As a result, an unstable state, i.e., a state in which

25    the phase error is not zero continues.

Fig. 8 is a block diagram showing a clock recovery and sampling circuit 121A and a synchronization judgment circuit 16B according to a second modified preferred embodiment of the present invention.   The

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second modified preferred embodiment is characterized by executing a synchronization judgment based on a phase error detected by the clock recovery and sampling circuit 121A.  In Fig. 8, the clock recovery and sampling circuit 121A includes a sampling circuit 61, a phase error

5   detector 62, a low-pass filter (LPF) 63 which is a loop filter, and a sampling timing signal generation circuit 64.

Referring to Fig. 8, the digital modulated signal inputted to the input terminal 120 shown in Fig. 2 is inputted to the sampling circuit 61. This inputted digital modulated signal is obtained by A/D converting one

10  modulated signal tuned and extracted by the QAM tuner 11 shown in Fig. 1 by an A/D converter (not shown) provided in a final stage of the QAM tuner 11.  A sampling timing at which the A/D converter performs A/D conversion is not a timing including the coding points for the received digital modulated signal.  Therefore, the sampling circuit 61 interpolates

15  the inputted digital modulated signal so as to include the coding points based on a sampling timing signal outputted from the sampling timing signal generation circuit 64, and performs clock recovery and sampling processings.  An output signal sampled so as to include the coding points for the inputted digital modulated signal by the sampling circuit 61 and

20  outputted from the sampling circuit 61 is outputted to the roll-off filter 122 provided in the subsequent stage of the clock recovery and sampling circuit 121A shown in Fig. 2, and is also outputted to the phase error detector 62.  The phase error detector 62 detects a sampling phase deviation (error) of the digital modulated signal outputted from the

25  sampling circuit 61, and outputs a voltage corresponding to the detected deviation (error) to the sampling timing signal generation circuit 64 through the LPF 63.  In response to this, the sampling timing signal generation circuit 64 generates a sampling timing signal based on the

voltage corresponding to the sampling timing phase error so that the voltage becomes zero and outputs the sampling timing signal to the sampling circuit 61.

The synchronization judgment circuit 16B time-averages the voltage being outputted from the phase error detector 62 and indicating the phase error of the sampling timing, and compares the average phase error with a predetermined threshold value. If the averaged value is smaller than the threshold value, then the synchronization judgment circuit 16B judges that the QAM demodulator 12 is synchronized with the QAM-modulated signal, and outputs a synchronization judgment result signal to the demodulation mode controller 17, the tuner frequency controller 18, and the apparatus controller 23, respectively.

If the coding point timing generated by the sampling timing signal generation circuit 64 includes the coding points for the inputted digital modulated signal, the phase error of the sampling timing detected by the phase error detector 62 becomes zero. If the coding point timing of the sampling timing signal generated by the sampling timing signal generation circuit 64 does not include the coding point for the inputted digital modulated signal, the phase error detector 62 detects and outputs the phase error.

In the clock recovery and sampling circuit 121A shown in Fig. 8, a negative feedback control loop is constituted so as to cancel the phase error of the sampling timing detected by the phase error detector 62. Therefore, a timing synchronized in phase with the coding point for the received digital modulated signal is reproduced and generated by the sampling timing signal generation circuit 64. This reproduced timing signal includes the coding points for the inputted digital modulated signal. The correct coding points can be thus obtained.

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By the way, if the baud rate indicated by the control signal outputted from the baud rate controller 170 to the sampling timing signal generation circuit 64 is adapted to the baud rate of the received digital modulated signal, then the phase error detector 62 can accurately detect

5    the phase error of the clock signal, and the negative feedback control loop functions so as to cancel the phase error. Therefore, the phase error detected by the phase error detector 62 becomes zero, finally. However, if the baud rate indicated by the control signal outputted from the baud rate controller 170 to the sampling timing signal generation circuit 64 is

10   not adapted to the baud rate of the received digital modulated signal, then the accurate timing phase error cannot be detected, and the negative feedback control loop does not operate normally. As a result, an unstable state, i.e., a state in which the phase error is not zero continues.

In the preferred embodiments mentioned above, the examples of

15   applying the present invention into the demodulation mode control using the STB 100 which receives the CATV broadcasting signal is described. However, the present invention is not limited to this   The present invention can be applied to the demodulation mode control over a digital modulated signal received through a predetermined transmission

20   medium, whether the medium is a wired or a radio medium.

Although the present invention has been fully described in connection with the preferred embodiments thereof with reference to the accompanying drawings, it is to be noted that various changes and modifications are apparent to those skilled in the art. Such changes and

25   modifications are to be understood as included within the scope of the present invention as defined by the appended claims unless they depart therefrom.